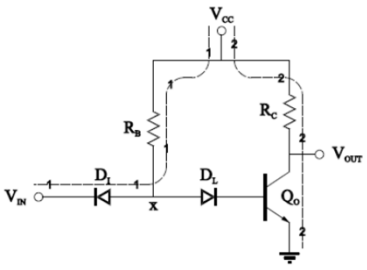
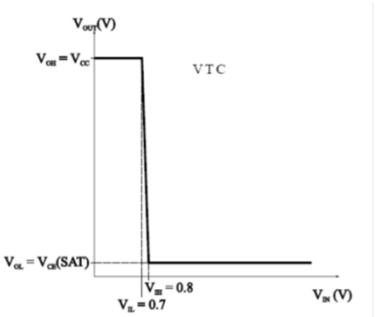
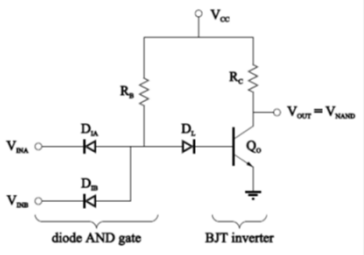
Diode-Transistor Logic
(DTL)

Basic DTL Inverter

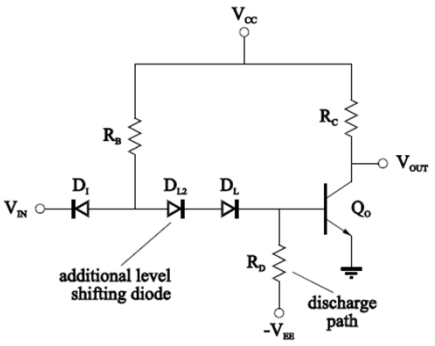


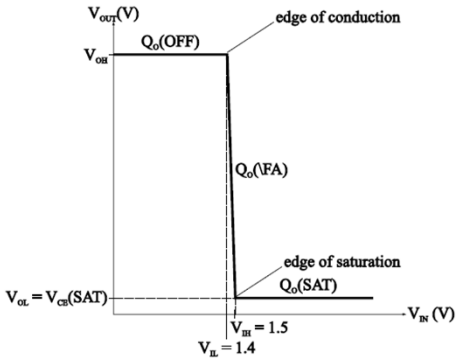


Basic DTL NAND Gate

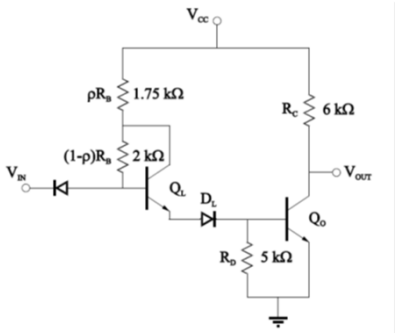


Diode Modified DTL Inverter





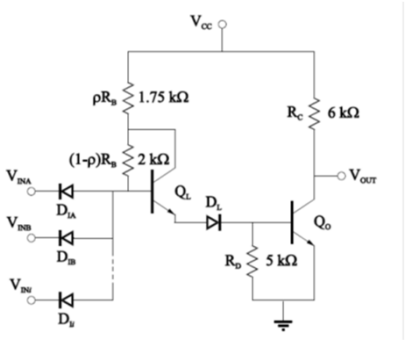
Transistor Modified DTL Inverter



Element	Purpose
D_1	Input diode, limits I_{IH}, and provides ANDing
ρR_B	Limits I_{IL}
$(1-\rho)R_B$	Self biases Q_L
Q_L	Base-emitter level-shifting for shift of transition width and provides base driving current to Q_O
D_L	Level-shifting diode for shift of transition width
R_D	Provides discharge path for saturation stored charge removal from base of Q_O
Q_O	Output inverting BJT and output low driver for current sinking pull-down
R_C	Passive current sourcing pull-up

Element	V_{OH}	V_{OL}
D_1	On	Cutoff
Q_L	Cutoff	Forward active
D_L	Cutoff	On
Q_O	Cutoff	Saturated

VTC of Transistor Modified DTL Inverter



$V_{OH} = V_{CC}$

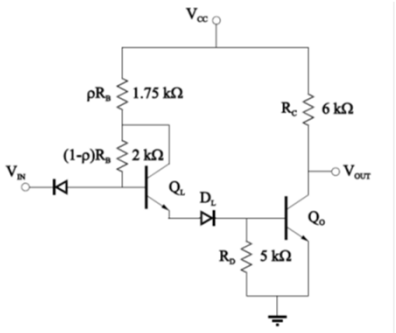
$V_{IL} = V_{BE,O(FA)} + V_{BE,L(FA)}$

$V_{OL} = V_{CE,O(SAT)}$

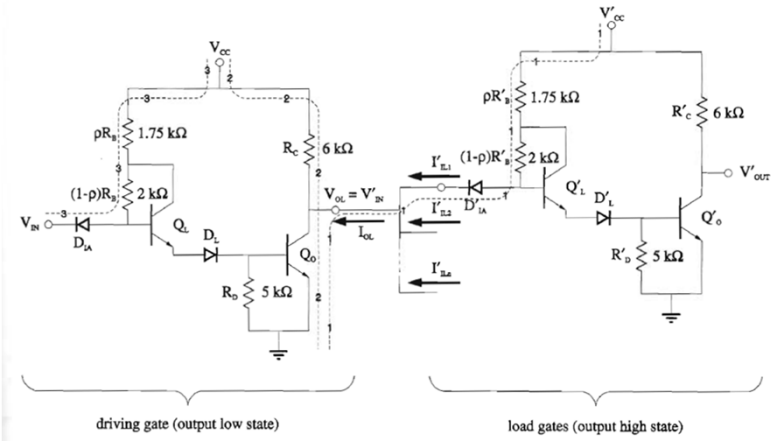
$V_{IH} = V_{BE,O(SAT)} + V_{BE,L(FA)}$

DTL Fan-out

Determined by the output low state as D_I is off for high-inputs



Cascaded DTL



$$I_{OL} = I_{C,O(SAT)} - I_{RC}$$

$$N = \left\lfloor \frac{I_{OL}}{I_{IL}} \right\rfloor$$

$$I_{RC} = \frac{V_{CC} - V_{CE,O(SAT)}}{R_C}$$

Path 2

$$I_{C,O(SAT)} = \sigma \beta_F I_{B,O(SAT)}$$

If not given (for maximum fan-out): $\sigma = 1$

$$I_{B,O} = I_{E,L} - I_{RD}$$

$$I_{RD} = \frac{V_{BE,O(SAT)}}{R_D}$$

$$I_{E,L} \cong \frac{V_{CC} - V_{BE,L(FA)} - V_{D,L(ON)} - V_{BE,O(SAT)}}{\rho R_B}$$

$$I_{IL} = \frac{V_{CC} - V_{D,1(ON)} - V_{CE,O(SAT)}}{R_B}$$

Path 3

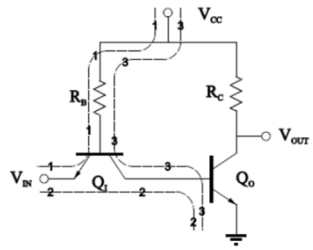
Example: Calculate the DTL fan-out for $\beta_F = 49$ and $\sigma = 0.85$.

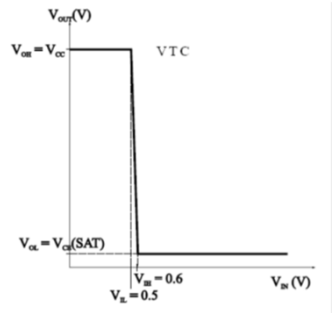
Power Dissipation

Example: Calculate the average power dissipation for the above example?

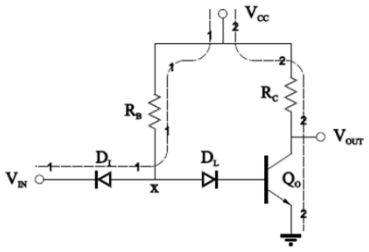
Tansistor-Transistor Logic
(TTL)

Basic TTL Inverter

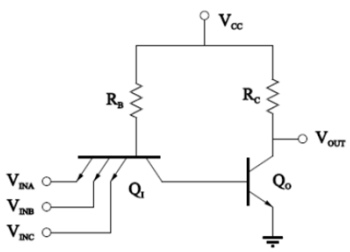




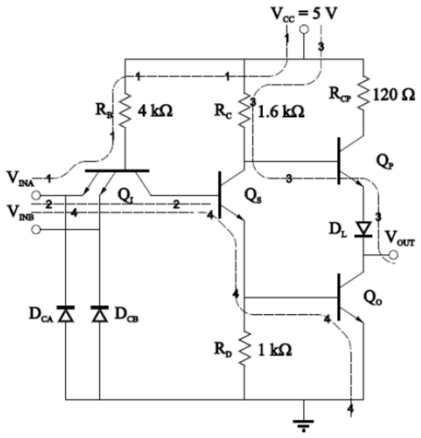
Basic DTL Inverter (compare)



Basic TTL NAND Gate

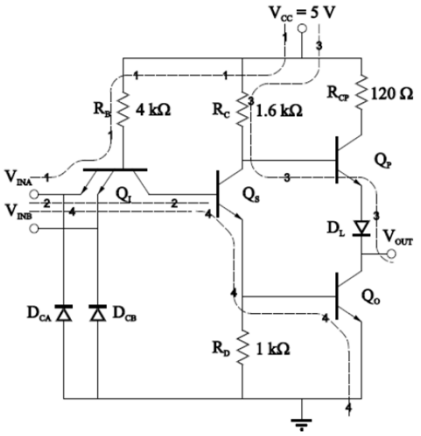


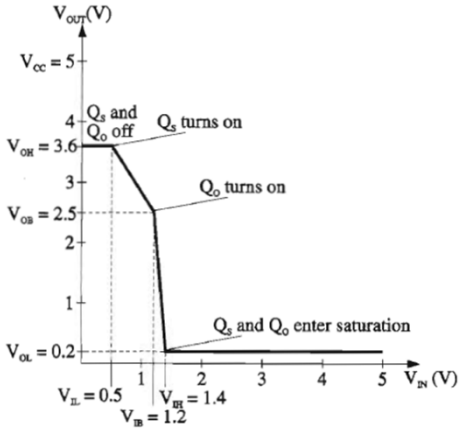
Actual TTL NAND Gate with Totem Pole Output



Element	Purpose
Q_I	Multi-emitter input BJT, base-collector level shifting of transition width, pull-down of Q_S
R_B	Limits I_{IL}
Q_S	Drive splitter, provides base driving current to Q_O, base-emitter level shifting for shift of transition width, pull-down of Q_P
R_C	Along with Q_S provides logic inversion to output-high driver
Q_O	Output inverting BJT, output low driver for current sourcing pull-down
D_L	Diode level shifting between V_{CC} and output
R_D	Provides discharge path for saturation stored charge of Q_O
Q_P	Provides active current-sourcing pull-up
R_{CP}	Part of active pull-up and limits current spikes during output high-to-low transitions
D_{C1}, D_{C2}	Input clamping diodes to limit the negative swing of the inputs to one diode drop below ground

VTC of an actual TTL Inverter





$$V_{OH} = V_{CC} - V_{BE,P(FA)} - V_{D,L(ON)}$$

$$V_{OL} = V_{CE,O(SAT)}$$

$$V_{OB} = V_{CC} - I_{RC}R_C - V_{BE,P(FA)} - V_{D,L(ON)}$$

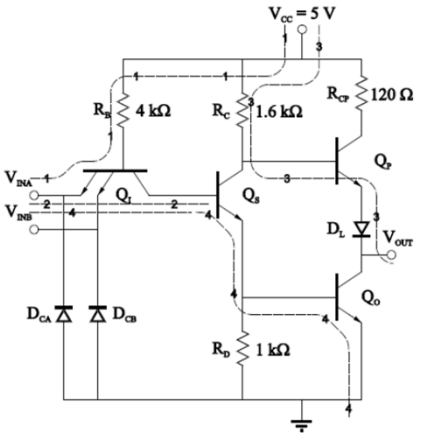
$$I_{RC} = I_{RD} = \frac{V_{BE,O(FA)}}{R_D}$$

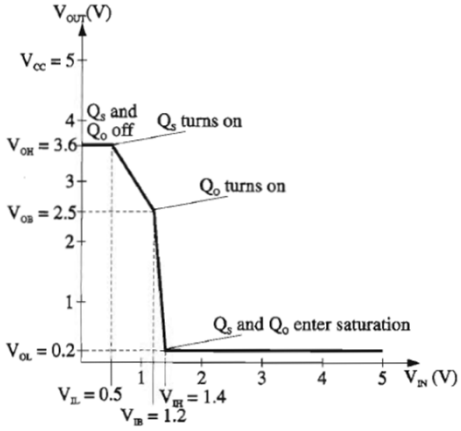
$$V_{IL} = V_{BE,S(FA)} - V_{CE,I(SAT))}$$

$$V_{IH} = V_{BE,O(SAT)} + V_{BE,S(SAT)} - V_{CE,I(SAT)}$$

$$V_{IB} = V_{BE,O(FA)} + V_{BE,S(FA)} - V_{CE,I(SAT)}$$

States of diodes and BJTs



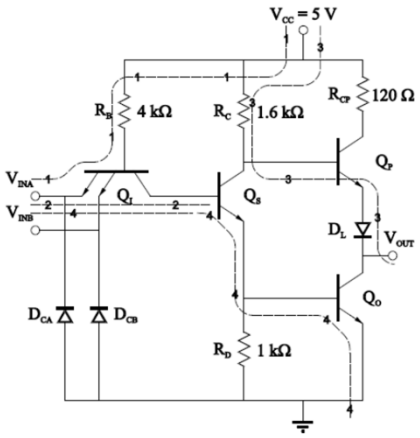


Element	V_{OH}	V_B	V_{OL}
Q_I	Saturated	Saturated	Reverse active
Q_S	Cutoff	Forward active	Saturated
Q_P	EOC	Forward active	Cutoff
D_L	EOC	EOC	Cutoff
Q_O	Cutoff	Edge of conduction	Saturated

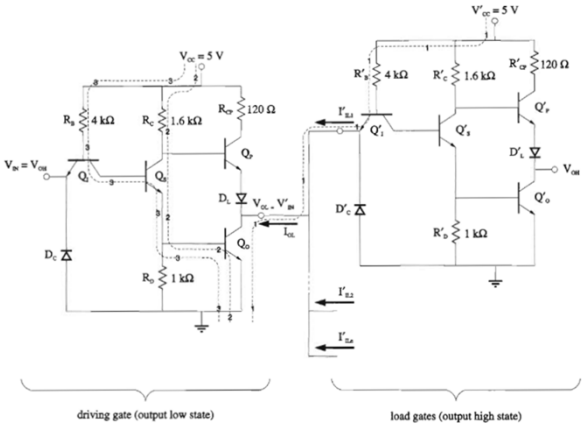
EOC: Edge of conduction

TTL Fan-out

Determined by the output low state as Q_I is cut-off for high-inputs



Cascaded TTL



Path 1

$$I_{IL} = \frac{V_{CC} - V_{BE,I(SAT)} - V_{CE,O(SAT)}}{R_B}$$

Path 2 & 3

$$I_{E,S(SAT)} = I_{B,S} + I_{C,S}$$

$$N = \left\lfloor \frac{I_{OL}}{I_{IL}} \right\rfloor$$

$$I_{OL} = I_{C,O(SAT)} = \sigma\beta_F I_{B,O(SAT)}$$

$$I_{B,O(SAT)} = I_{E,S(SAT)} - I_{RD}$$

$$I_{RD} = \frac{V_{BE,O(SAT)}}{R_D}$$

Unless given $\sigma = 1$

$$I_{C,S} = \frac{V_{CC} - V_{CE,S(SAT)} - V_{BE,O(SAT)}}{R_C}$$

$$I_{B,S} = I_{C,I(RA)} = (1+\beta_R) I_{B,I}$$

$$I_{B,I} = \frac{V_{CC} - V_{BC,I(RA)} - V_{BE,S(SAT)} - V_{BE,O(SAT)}}{R_B}$$

Example (TTL Fan-out)

Example: Calculate the TTL fan-out for $\beta_F = 25$, $\sigma = 0.85$ and $\beta_R = 0.1$

$I_{RB(OL)} = 675\ \mu A$ $\quad I_{IL} = I_{RB(OH)} = 1\ mA$

$I_{RC(OL)} = 2.5\ mA$ $\quad I_{OL} = 51.9\ mA$

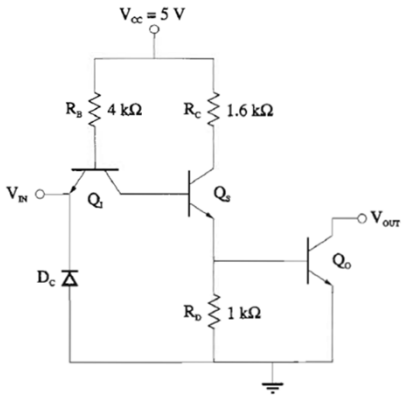
$$N = \left\lfloor \frac{I_{OL}}{I_{IL}} \right\rfloor = 51$$

Example (Power Dissipation)

Example: Calculate the average power dissipation for the above example?

$P_{CC(avg)} = 10.4\ mW$

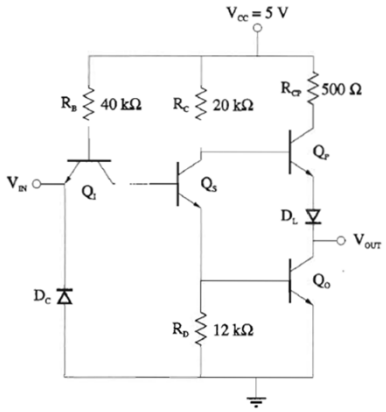
Open-Collector TTL



Mostly used in data busses where multiple gate outputs must be ANDed.

- This can be accomplished by using a single pull-up resistor with open-collector TTL gates
- This type of connection is referred to as *wired-AND*.

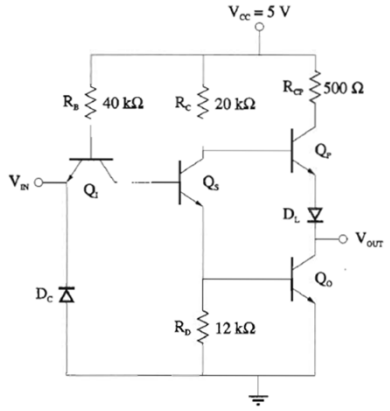
Low Power TTL (LTTL)



Accomplished simply by increasing the resistance values. However this results in

- Decreased fan-out
- Longer transient-response times

LTTL Example



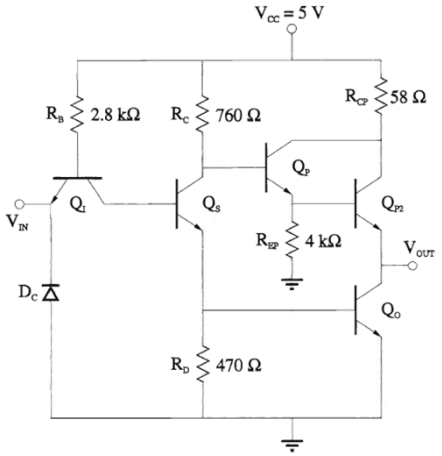
Compare the power dissipation of the LTTL and TTL gates.

$I_{RB(OL)}$ = 67.5 μA $I_{RB(OH)}$ = 100 μA $P_{CC(avg)}$ = 919 μW

$I_{RC(OL)}$ = 200 μA

TTL vs LTTL power dissipation ratio = 10.4 / 0.919 = 11.3

High Speed TTL (HTTL)



Accomplished simply by decreasing the resistance values. However this results in

- Increased power dissipation

Speed & Power Relationship

Family	Power	Prop. Delay
TTL	10 mW	9 ns
STTL	20 mW	3 ns
LSTTL	2 mW	9 ns
ASTTL	10 mW	2 ns
ALSTTL	1 mW	4 ns
FAST	4 mW	2 ns